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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT; PLUR=YES; OP=OR		
L16	L15 and l13	9	L16
L15	L11 same ((data or card or chip or module) near4 (secur$4 or protect$4 or prevent$4 or remov$4 or eras$4 or delet$4))	4581	L15
L14	L13 and ((latch or flip-flop or register or nonvolatile or non-volatile) with ((data or card or chip or module) near4 (secur$4 or protect$4 or prevent$4 or remov$4 or eras$4 or delet$4)))	14	L14
L13	L12 and (((alternate or independent or separate) near6 (voltage or current or power or dc)) same battery)	94	L13
L12	L11 and l6	5853	L12
L11	((latch or flip-flop or register or nonvolatile or non-volatile) near4 (state or set$3 or reset$3 or initializ$4 or high or low or "1" or "0"))	189470	L11
L10	L8 and (((alternate or independent or separate) near6 (voltage or current or power or dc)) same battery)	86	L10
L9	L8 and (((alternate or independent or separate) near6 (voltage or current or power)) same battery)	80	L9
L8	L7 and l6	4248	L8
L7	((latch or flip-flop or register or nonvolatile or non-volatile) near4 (state or set$3 or reset$3 or initializ$4))	128453	L7
L6	(hardware or embedded or key) near4 (secur$4 or protect$4 or prevent$4)	47569	L6
L5	(hardware or embedded) near4 (secur$4 or protect$4 or prevent$4)	16487	L5

L4	l2 and l3	16	L4
L3	((latch or flip-flop or register or nonvolatile) near4 (set$3 or reset$3 or initializ$4))	106522	L3
L2	l1 and (battery and ((remov$5 or detach$5 or dismount$4 or disconnect$4) near4 (chip or card or planar or motherboard)))	67	L2
L1	(365/226-229.ccls.)	2824	L1

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L10 and L8	0

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Search: L11

Refine Search

Recall Text Clear Interrupt

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	DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L11	L10 and l8	0	L11
L10	L9 same (signal near4 (remov$4 or interrupt$3 or disconnect$3 or detach$3 or dismount$3))	2111	L10
L9	(latch or flip-flop or register or nonvolatile) near4 (set$3 or reset$3 or initializ$4)	56333	L9
L8	(battery near6 signal) with (system near4 (power or current or voltage))	302	L8
	DB=PGPB,USPT; PLUR=YES; OP=ADJ		
L7	L6 and l1	1	L7
L6	L5 and l2	16	L6
L5	L3 same (signal near4 (remov$4 or interrupt$3 or disconnect$3 or detach$3 or dismount$3))	5337	L5
L4	L3 same l2	7	L4
L3	(latch or flip-flop or register or nonvolatile) near4 (set$3 or reset$3 or initializ$4)	106522	L3
L2	(battery near6 signal) with (system near4 (power or current or voltage))	931	L2
L1	365/226-229.ccls.	2824	L1

Refine Search

Search Results -

Terms	Documents
((charg$3 near3 pump) near8 (power or current or voltage or dc)) with ((remov$4 or detach$4 or dismount$4) near8 (card or chip or board or medium))	0

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Search: L4

Refine Search

Recall Text   Clear   Interrupt

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Set Name side by side	Query	Hit Count	Set Name result set
	DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L4	((charg$3 near3 pump) near8 (power or current or voltage or dc)) with ((remov$4 or detach$4 or dismount$4) near8 (card or chip or board or medium))	0	L4
	DB=PGPB,USPT; PLUR=YES; OP=ADJ		
L3	((charg$3 near3 pump) near8 (power or current or voltage or dc)) with ((remov$4 or detach$4 or dismount$4) near8 (card or chip or board or medium))	3	L3
L2	L1 with (power or current or voltage or dc)	1430	L2
L1	(charg$3 near3 pump) with (card or chip or board or detach$4 or remov$4 or dismount$4 or mount$4)	2233	L1

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Term:

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

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DATE: Saturday, July 24, 2004 Printable Copy Create Case

Set Name side by side	**Query**	**Hit Count**	**Set Name** result set
	DB=PGPB,USPT; PLUR=YES; OP=OR		
L4	l2 and l3	16	L4
L3	((latch or flip-flop or register or nonvolatile) near4 (set$3 or reset$3 or initializ$4))	106522	L3
L2	l1 and (battery and ((remov$5 or detach$5 or dismount$4 or disconnect$4) near4 (chip or card or planar or motherboard)))	67	L2
L1	(365/226-229.ccls.)	2824	L1

END OF SEARCH HISTORY

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1 From Electron Mobility to Logical Structure: A View of Integrated Circuits
Wesley A. Clark
September 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 3
Full text available: pdf(3.29 MB) Additional Information: full citation, references, citings, ind

2 Pen computing: a technology overview and a vision
André Meyer
July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3
Full text available: pdf(5.14 MB) Additional Information: full citation, abstract, citing

This work gives an overview of a new technology that is attracting growing interest in public as we other technologies is in the use of a pen or pencil as the primary means of interaction between a u metaphor. From this follows a set of consequences that will be analyzed and put into context with historic ...

3 Design strategies for active power reduction: Energy recovery clocking scheme and flip-flops
Matthew Cooke, Hamid Mahmoodi-Meimand, Kaushik Roy
August 2003 **Proceedings of the 2003 international symposium on Low power electroni**
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A significant fraction of the total power in highly synchronous systems is dissipated over clock netv approaches for future designs. We propose four novel energy recovery flip-flops that enable energ savings. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be genera 0.25mm CM ...

Keywords: adiabatic, clock, clock tree, energy recovery, flip-flop

4 Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation
Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Rajeev Rao, Toan Pham, Conrad Ziesler, D
December 2003 **Proceedings of the 36th Annual IEEE/ACM International Symposium on M**
Full text available: pdf(568.17 KB) Publisher Site Additional Information: full citation, abstract, index

With increasing clock frequencies and silicon integration,power aware computing has become a cri chip.One of the more effective and widely used methods for power-awarecomputing is dynamic vo from DVS, it is essentialto scale the supply voltage as low as possible while ensuringcorrect operat worst-case ...

5 Energy- w re design of embedded memories: A survey of technologies, rchitectures, nd

Luca Benini, Alberto Macii, Massimo Poncino
February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available: pdf(288.44 KB) Additional Information: full citation, abstract, refere

Embedded systems are often designed under stringent energy consumption budgets, to limit heat significant amount of energy to store and to forward data, it is then imperative to balance power c Contemporary system design focuses on the trade-off between performance and energy consumpt interconnections. Although memory design is as ...

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile, systerr

6 Testing: Low-power weighted pseudo-random BIST using special scan cells
Shalini Ghosh, Eric MacDonald, Sugato Basu, Nur A. Touba
April 2004 **Proceedins of the 14th ACM Great Lakes symposium on VLSI**

Full text available: pdf(115.91 KB) Additional Information: full citation, abstract, refere

In this paper, a technique for weighted pseudo-random built-in self-test (BIST) of VLSI circuits is | algorithm to achieve low power dissipation. It is based on weighted pseudo-random scan testing ir random value (0.5). A new weight selection algorithm is used to select a set of weights that achie minimize ...

Keywords: built-in self-test, low power, weighted pseudo-random testing

7 Teaching digital logic design using a tape recorder simulator
R. P. Srivastava
February 1990 **Proceedings of the 1990 ACM SIGSMALL/PC symposium on Small systems**

Full text available: pdf(658.62 KB) Additional Information: full citation, abstract, refere

This paper describes two implementations of a tape recorder simulator. One is based on hard-wire approach. Both implementations are compared and evaluated for such points as flexibility, speed, is to introduce students of digital logic design to the problems of selecting a suitable implementati constraints. This is ...

8 Very rapid prototyping of wearable computers: a case study of custom versus off-the-shelf d
Asim Smailagic, Daniel P. Siewiorek, Richard Martin, John Stivoric
June 1997 **Proceedings of the 34th annual conference on Design automation**

Full text available: pdf(121.36 KB) Additional Information: full citation, references, index terms

9 Synthesis and simulation of digital systems containing interacting hardware and software coı
R. K. Gupta, C. N. Coelho, G. De Micheli
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(789.92 KB) Additional Information: full citation, references, citings, index terms

10 Compressionless routing: a framework for adaptive and fault-tolerant routing
J. H. Kim, Z. Liu, A. A. Chien
April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST anr**
Volume 22 Issue 2

Full text available: pdf(1.17 MB) Additional Information: full citation, abstract, refere

Compressionless Routing (GR) is a new adaptive routing framework which provides a unified fram tolerance. CR exploits the tight-coupling between wormhole routers for flow control to detect pote Compressionless Routing (FCR) extends Compressionless Routing to support end-to-end fault-tole complexity and performance sim ...

11 A Survey of Microcellul r Rese rch

Robert C. Minnick
April 1967 **Journal of the ACM (JACM)**, Volume 14 Issue 2

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This paper is a survey of research on microcellular techniques. Of particular interest are those tecl fabrication processes, since the rapid emergence of reliable and economical batch-fabricated comp field of digital circuits. First the manufacturing methods for batch-fabricated components are revie

12 Microprocessor applications in the nuclear industry
C. Dwayne Ethiridge
April 1980 **ACM SIGCAS Computers and Society**, Volume 10 Issue 3-4

Full text available: pdf(986.50 KB) Additional Information: full citation, abstract, refere

Microprocessors in the nuclear industry, particularly at the los Al amos Scientific Laboratory, have from data acquistion and control for basic physics research to monitoring special nuclear material to support weapons diagnostics measurements during undergorund weapons testing at the Nevad controlling ...

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